BEE 332 Lab 4
Multistage amplifiers
Spring 2017

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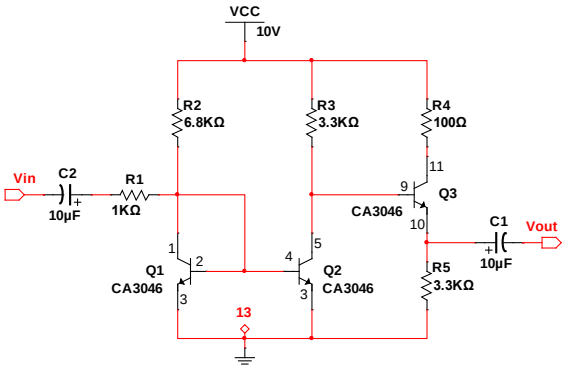
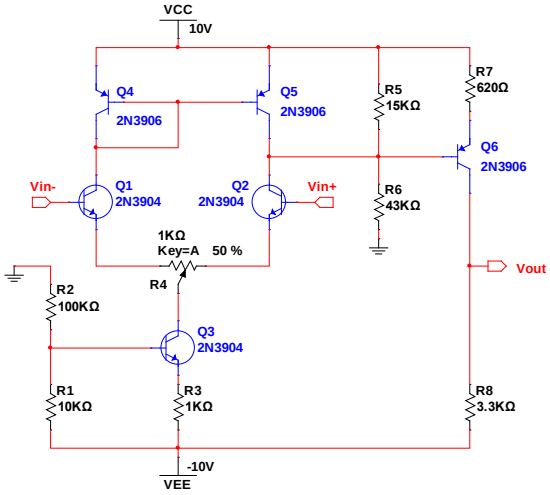
https://faculty.washington.edu/kd1uj

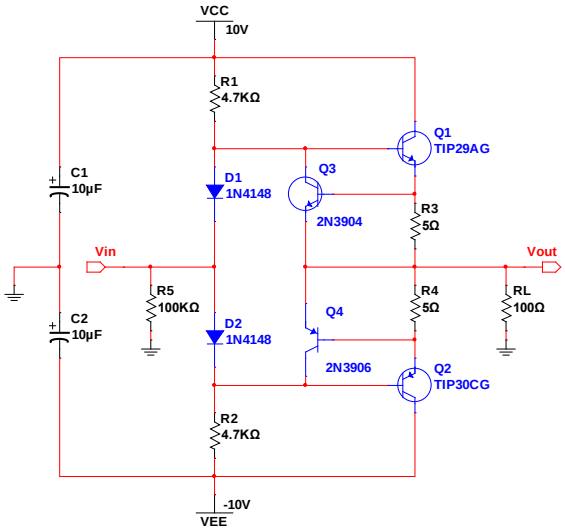
Four circuits



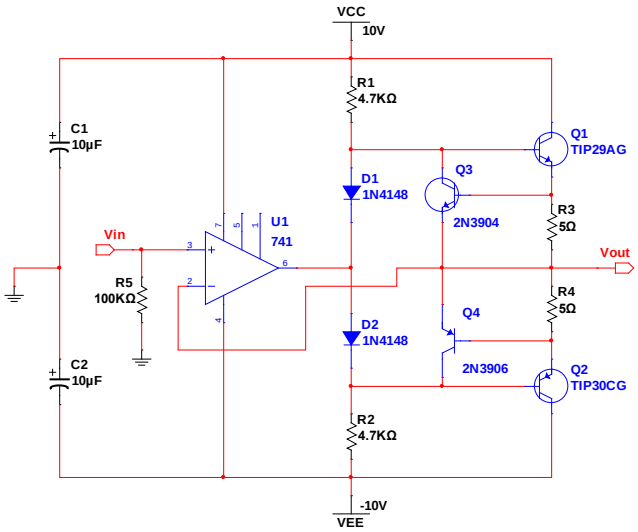
Wideband CE-EF amplifier.



A simple opamp.

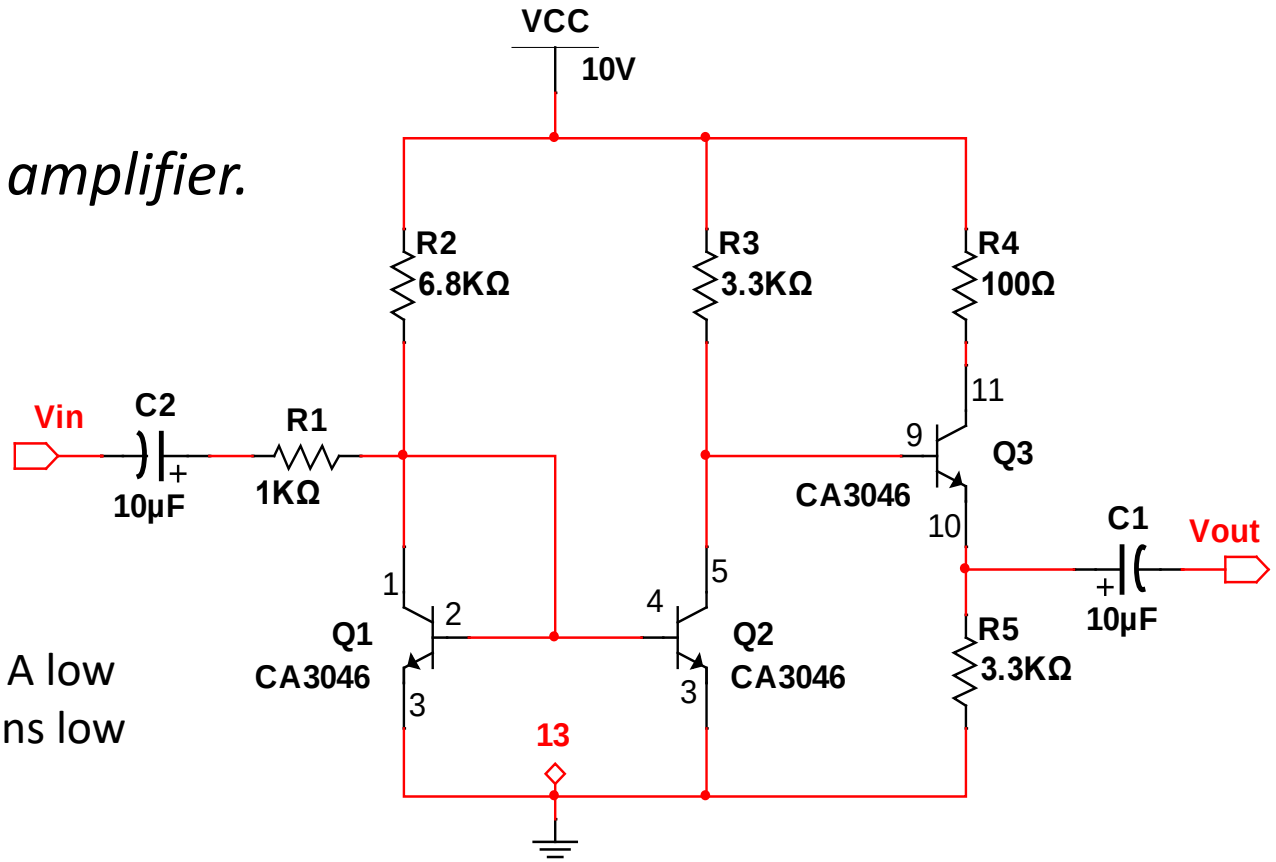


Complementary class AB output stage.



Multi-stage amplifier with feedback.

Wideband CE-EF amplifier.

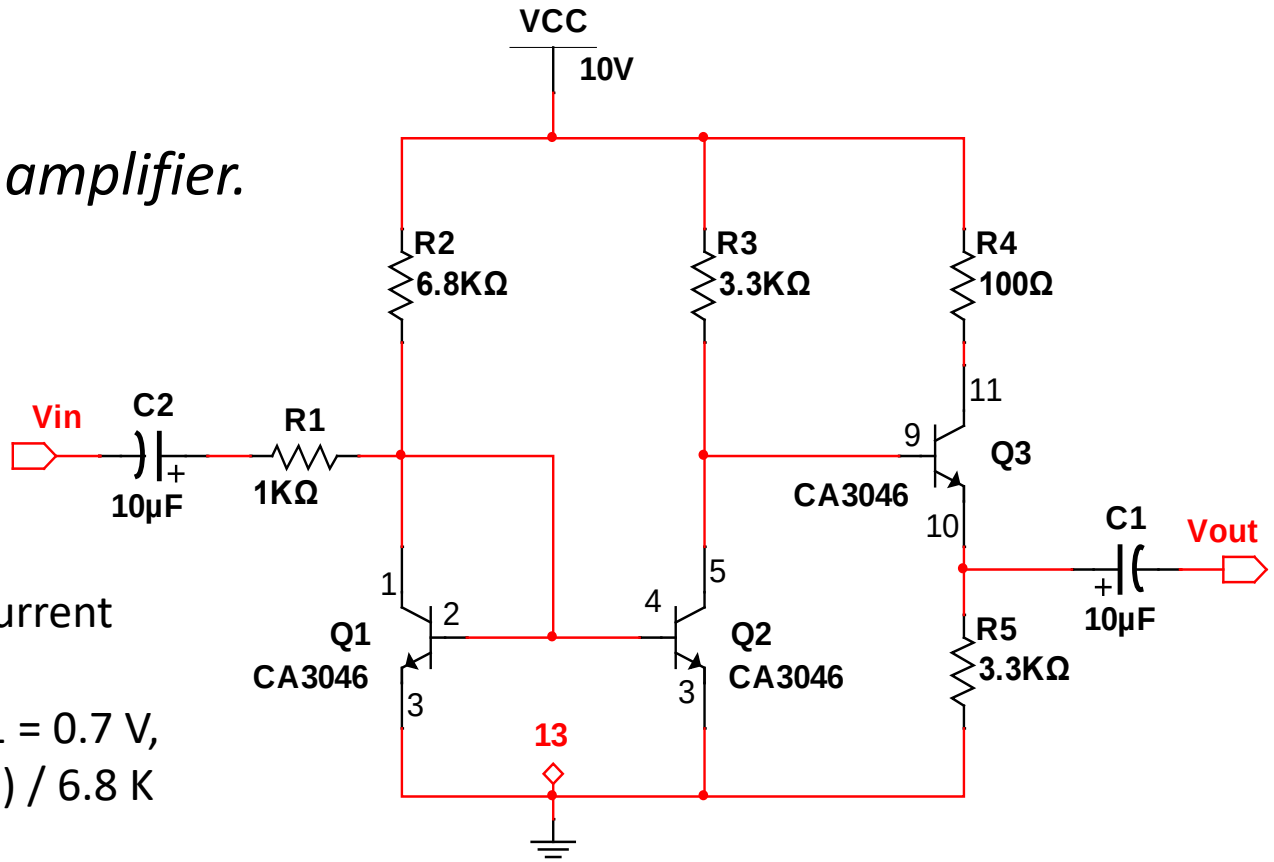


Av for a CE circuit is proportional to RC. A low resistance load means low Av.

One solution is a second emitter follower stage, which offers only unity Av, but Ai = β + 1

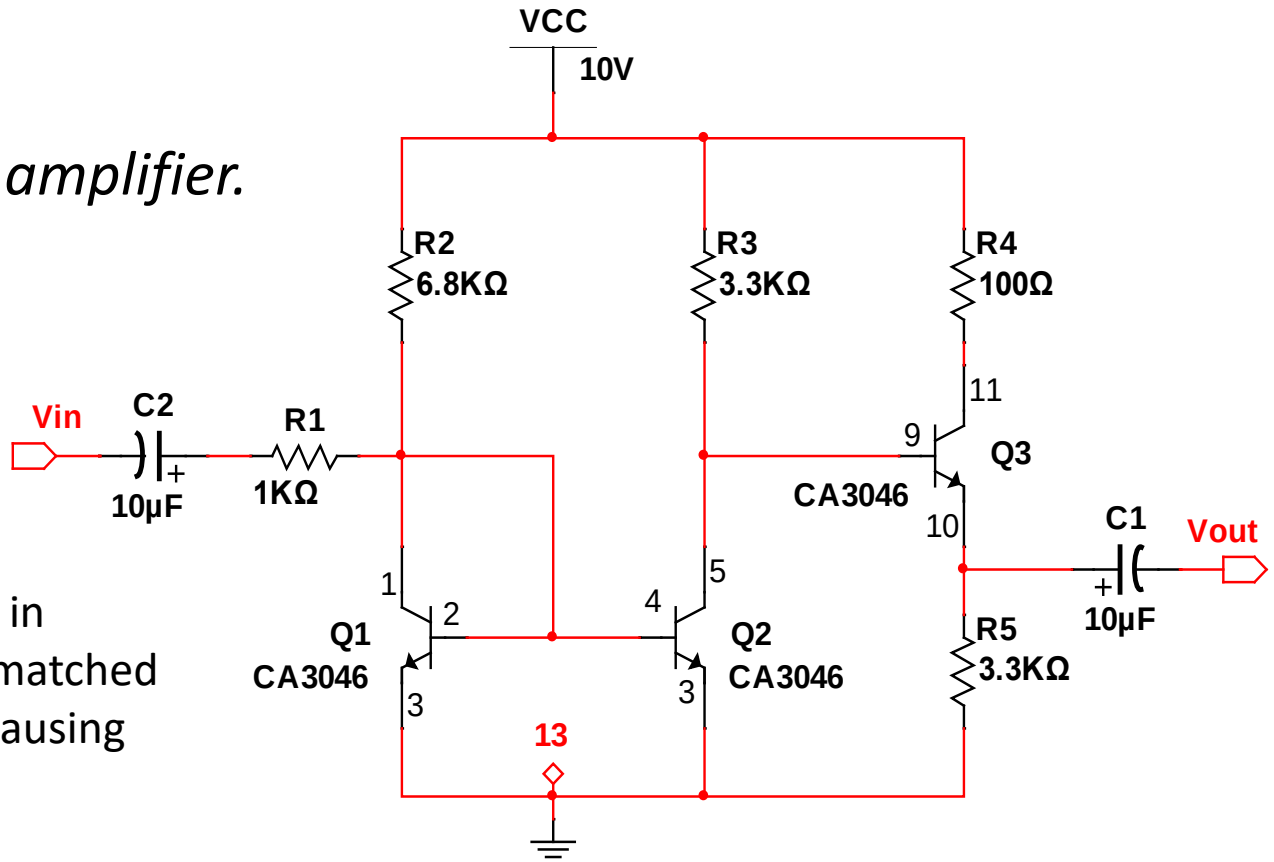
The Q1-Q2 pair is a current mirror, used here to bias Q2..
Whatever the value of IC1, IC2 = IC1.
Av ~= R3/R1.

Wideband CE-EF amplifier.



Q1 and Q2 form a current mirror.
With expected VCE1 = 0.7 V, Iref = IR2 = (10 – 0.7) / 6.8 K = 1.4 mA.
Assuming Iref ≅ IC1, IR3 will be about the same, meaning VB3 = 10 – 3.3K * 1.4 mA = 5.38 V.
Quiescent VE3 should be about 5.4 – 0.7 = 4.7 V.

Wideband CE-EF amplifier.



Both Q1 and Q2 are in forward active and matched with VBE1 = VBE2, causing IC1 = IC2.

If we inject a small additional current into IC1, it will be matched in IC2.

Since VBE can be assumed constant at 0.7 V, we can ignore R2.

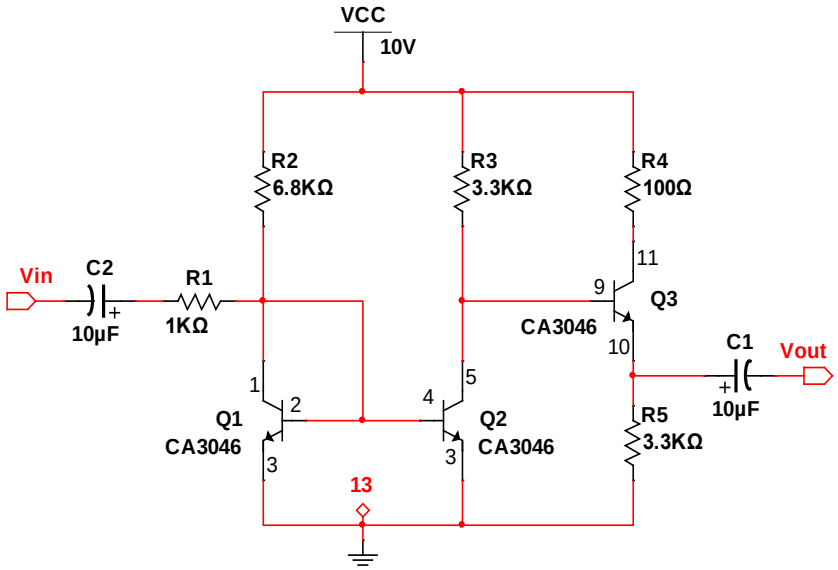
$$\Delta Iref = \frac{\Delta Vin}{R1} \cong \Delta IC1 = \Delta IC2 \cong \Delta IR3$$

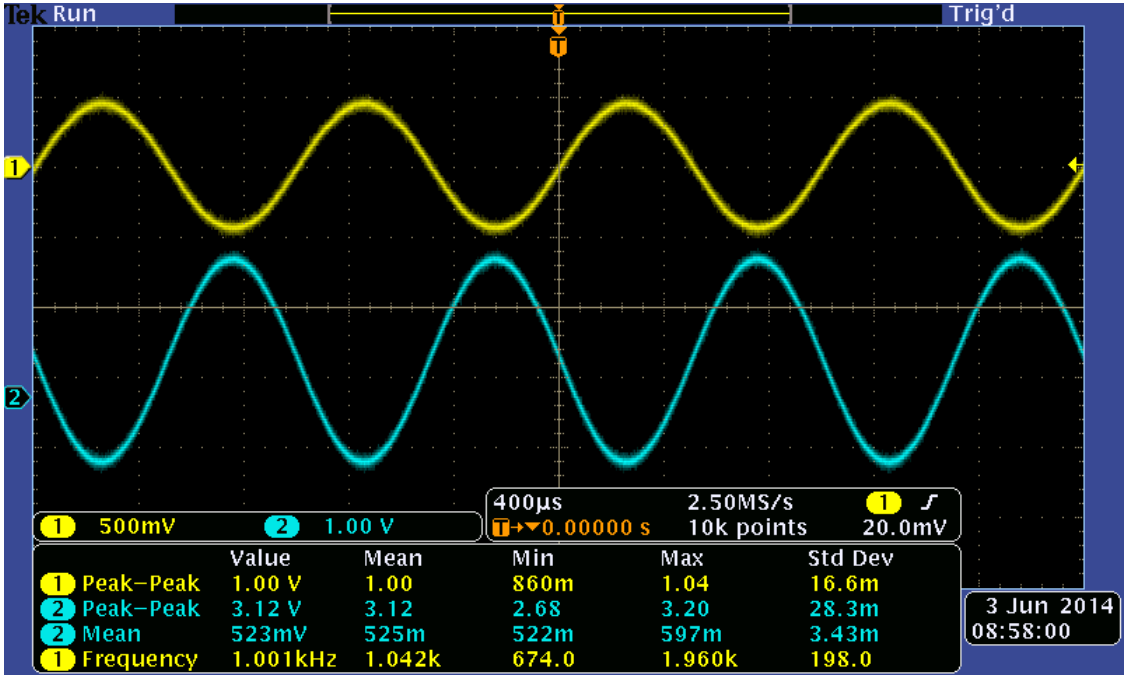
$$\Delta VC2 = -R3 * \Delta IR3 = -R3\left(\frac{\Delta Vin}{R1}\right) = -\left(\frac{R3}{R1}\right)\Delta Vin$$

$$Av = \frac{\Delta VC2}{\Delta Vin} = -\frac{R3}{R1}$$

Measurements: Gain

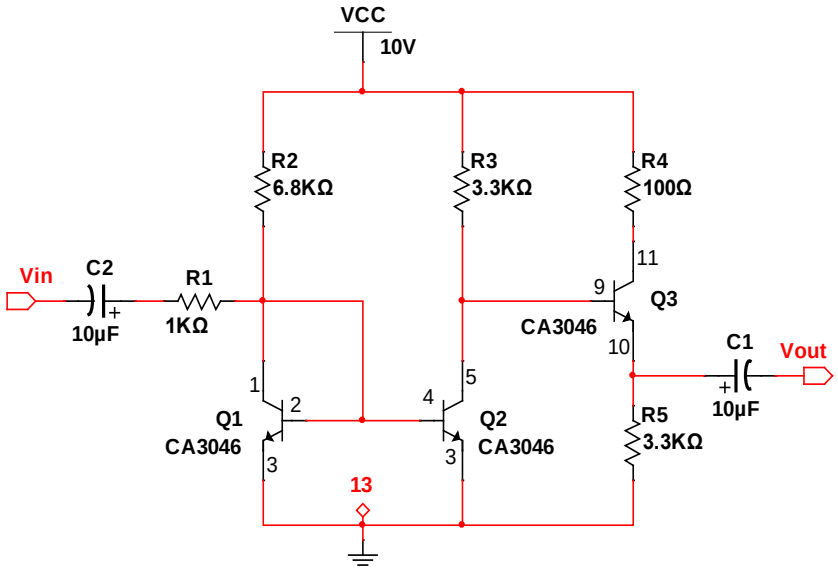
1. Set Vin = 1 Vpp, 1.0 KHz sine wave, 0 V DC offset.
2. Capture an oscilloscope screenshot.
3. Calculate gain. For me, Av = 3.12.

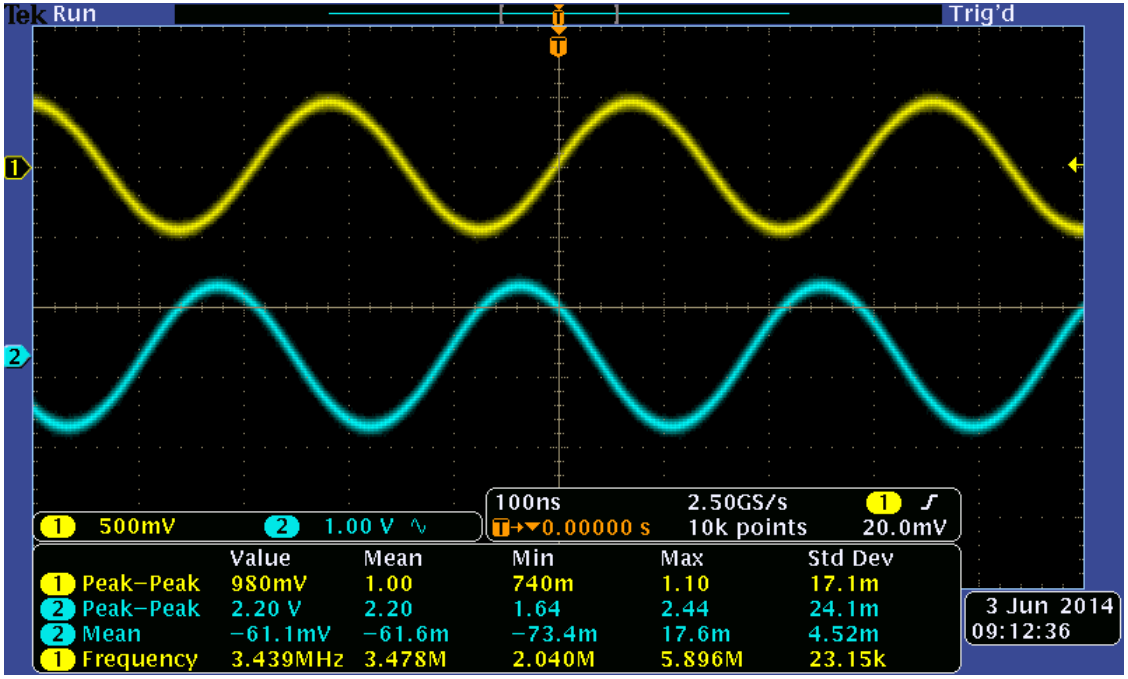




Measurements: Bandwidth

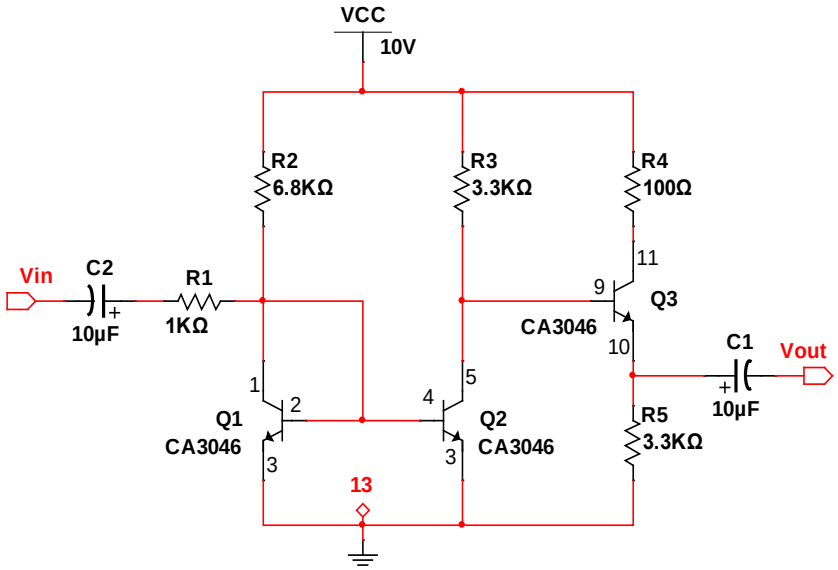
1. Increase frequency until Av has fallen by 3 dB.
2. Capture an oscilloscope screenshot.
3. For me, Av = 2.20 at 3.5 MHz.

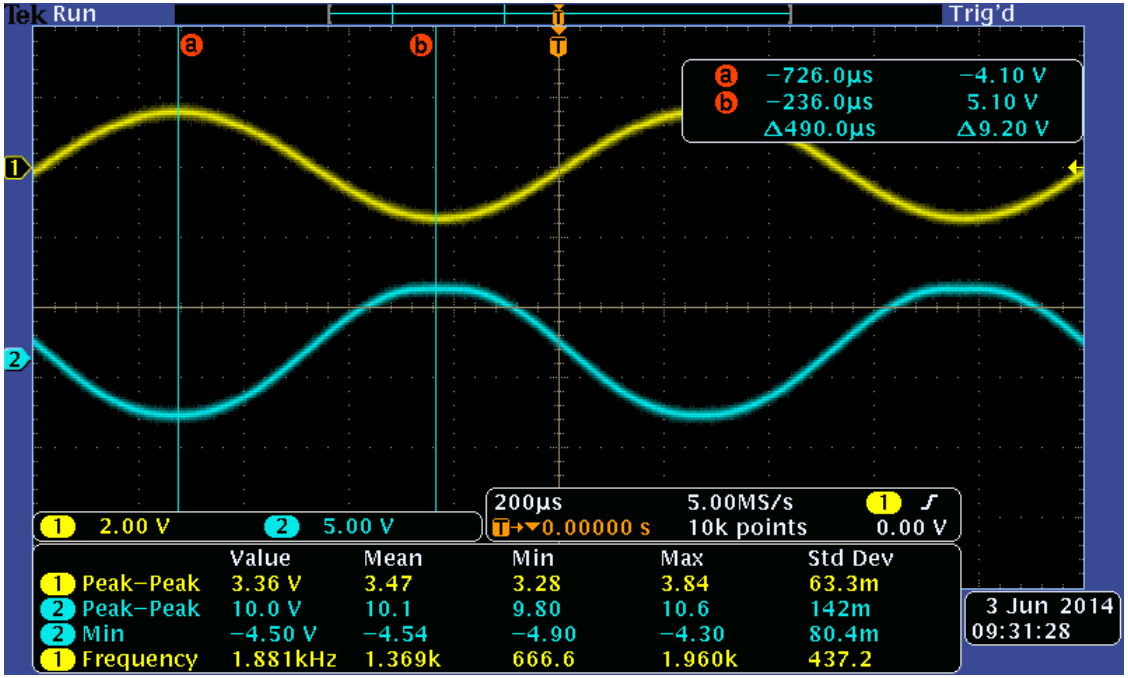




Measurements: Onset of clipping

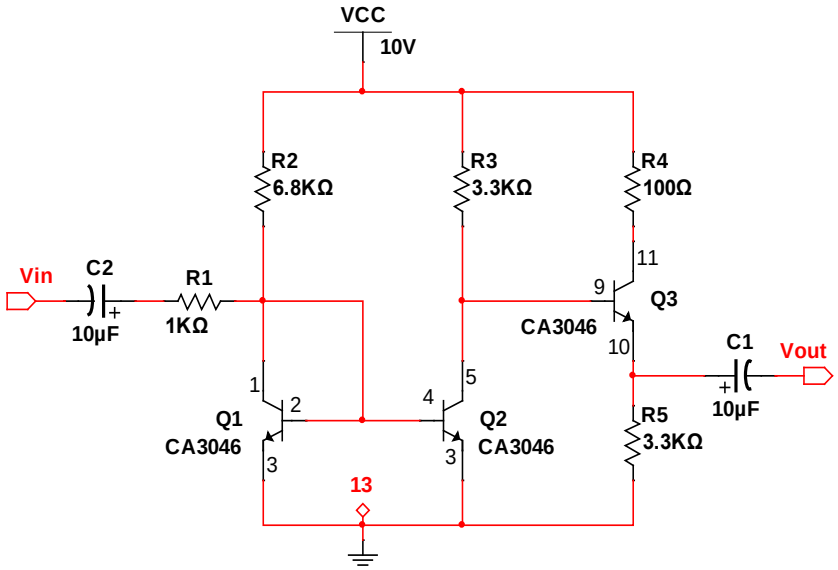
1. Set Vin = 1 Vpp, 1.0 KHz sine wave, 0 V DC offset .
2. Increase amplitude until onset of clipping.
3. Capture an oscilloscope screenshot.
4. For me, Vin = 3.47 Vpp and Vout = 10.1 Vpp.

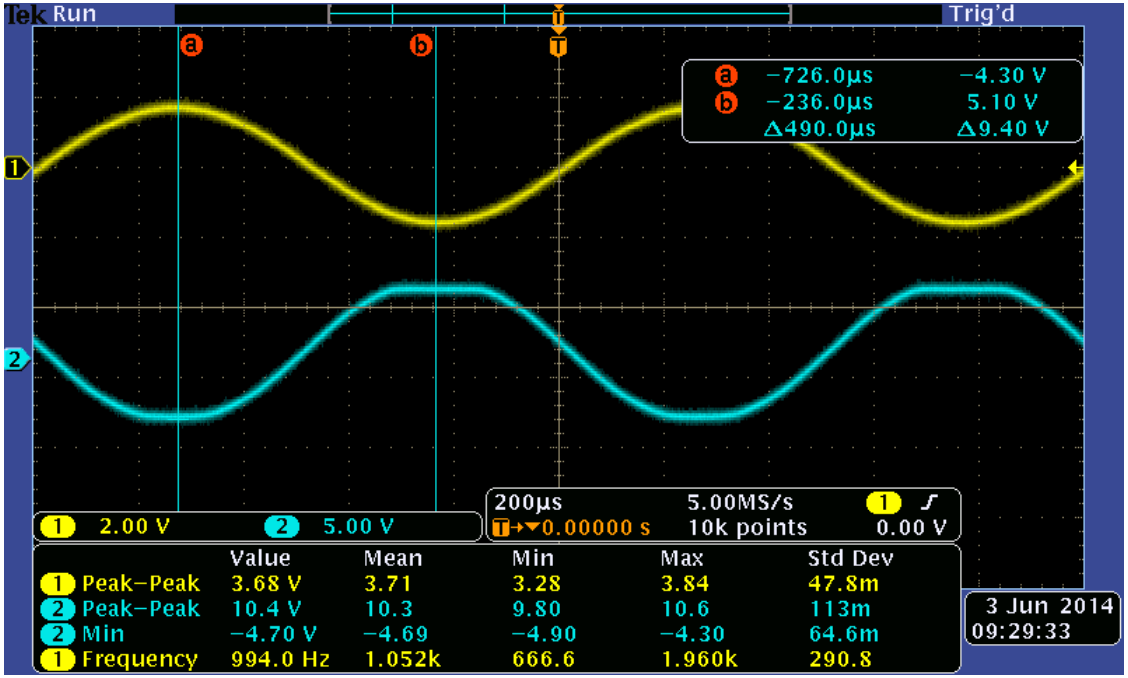




Measurements: Clipping both peaks

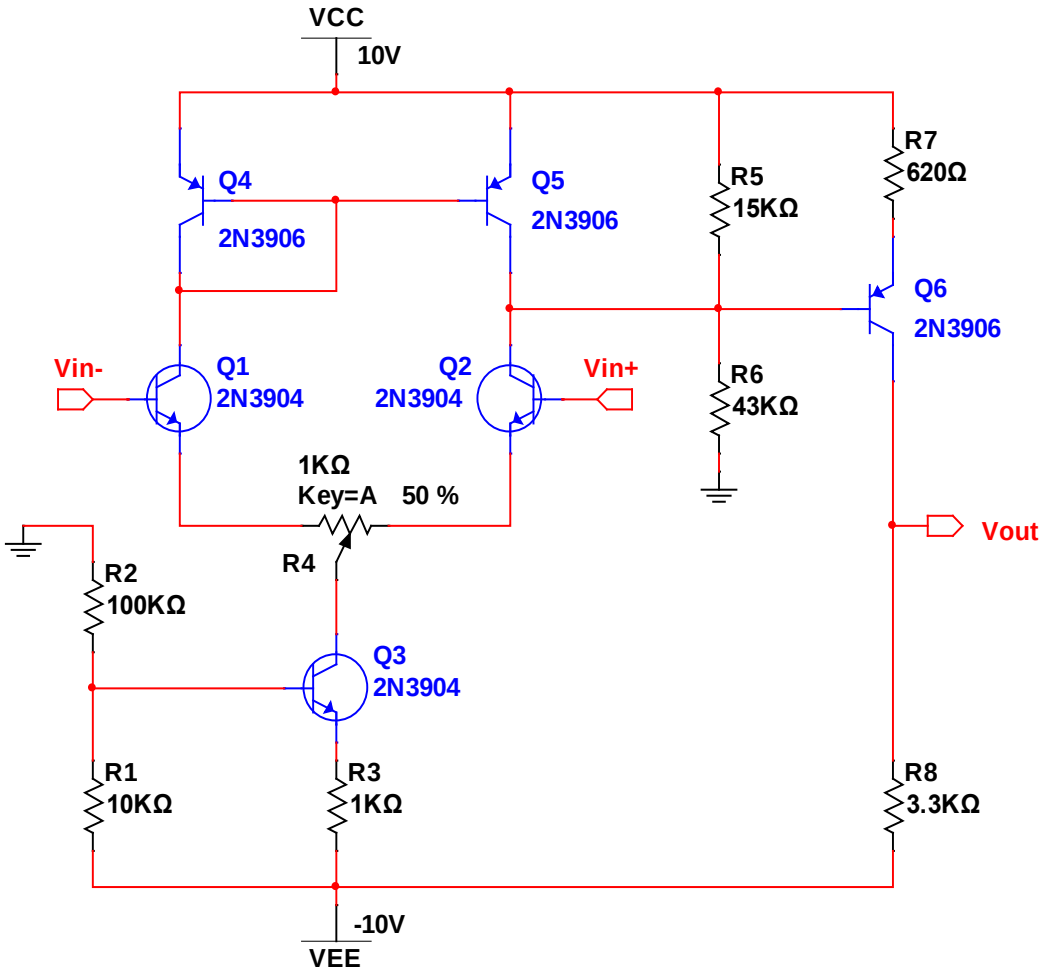
1. Increase amplitude until clipping on both peaks.
2. Capture an oscilloscope screenshot.
3. For me, Vin = 3.71 Vpp and Vout = 10.3 Vpp.





A simple opamp.

An active load usually refers to the use of a transistor as the output load for a common-emitter stage, greatly increasing the voltage gain since the collector resistance for the CE amplifier stage is now the output resistance of the active load transistor.

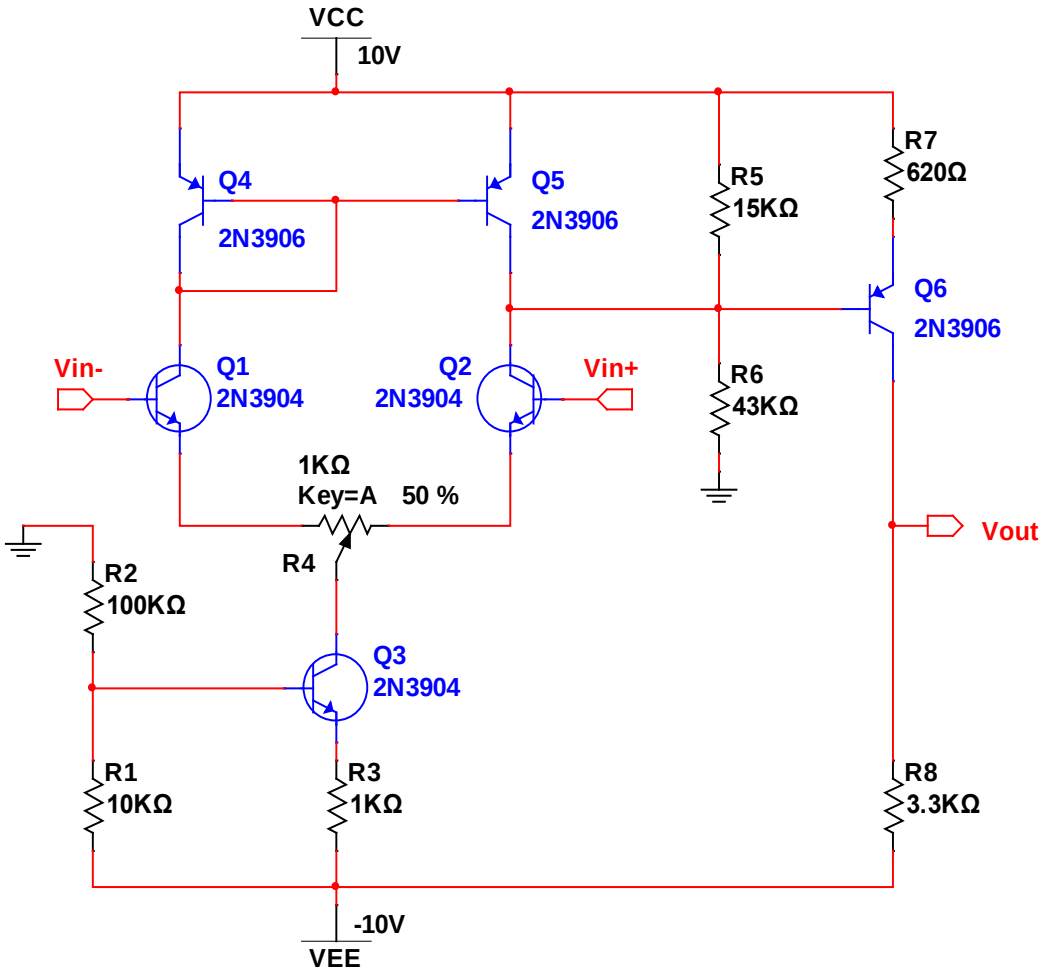


A simple opamp.

Q3 provides a current source for the differential pair.

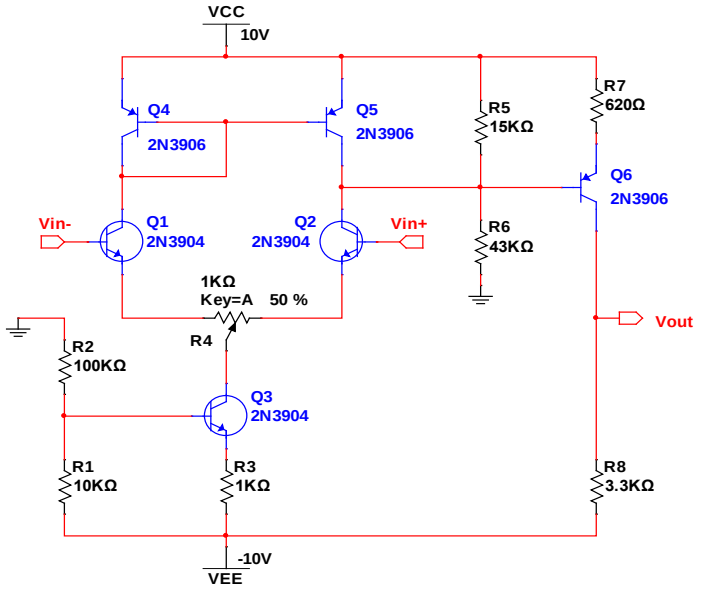
Q6 is a simple PNP CE stage.

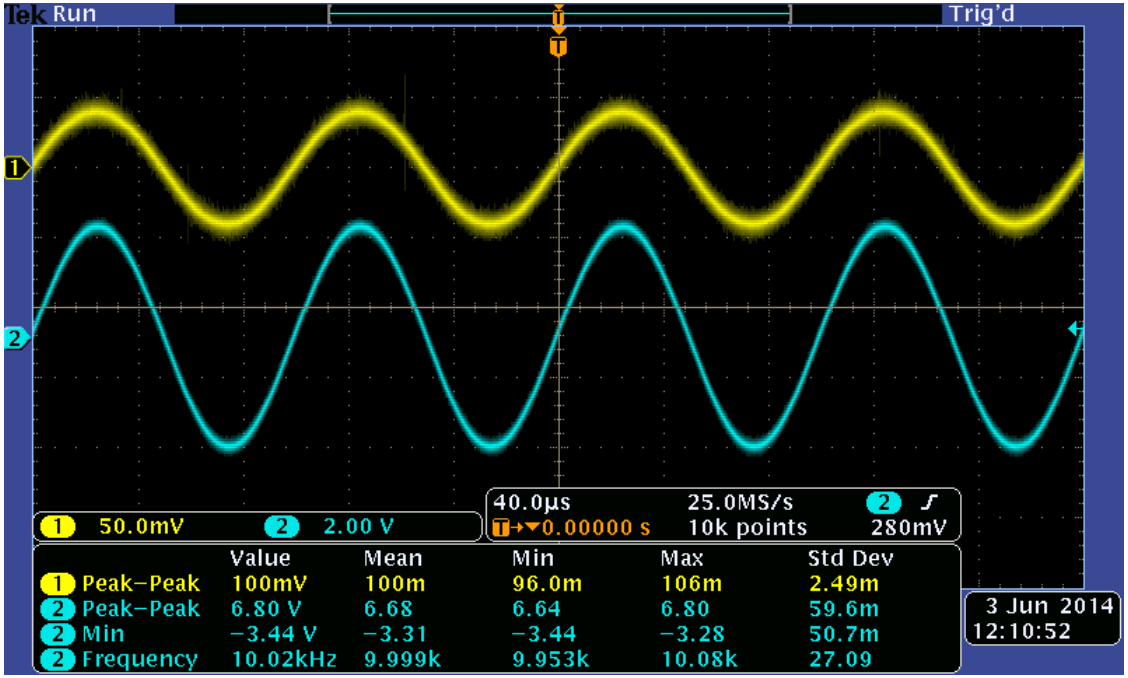
R4 is an optional trimpot to allow the differential pair to be balanced so the output is zero when the differential input is zero. But it lowers the gain.



Measurements: Gain

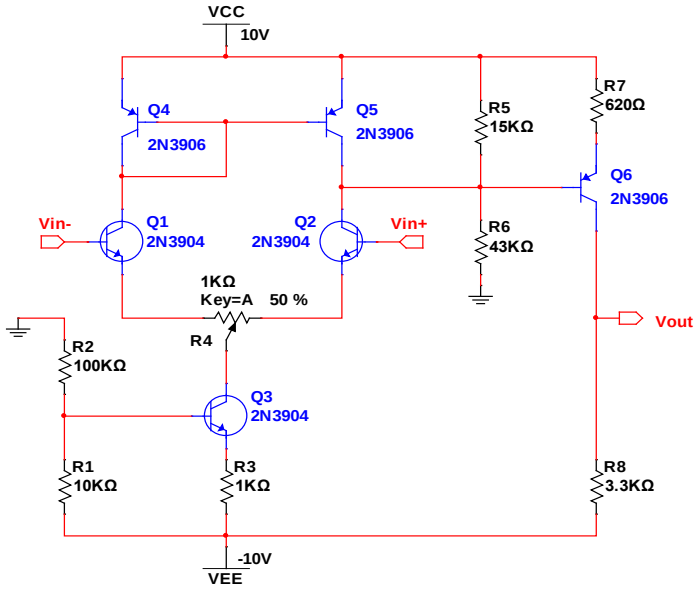
1. Set Vin = 100 mVpp, 1.0 KHz sine wave, 0 V DC offset.
2. Capture an oscilloscope screenshot.
3. Calculate gain. For me (at 10 KHz), Av = 66.8.
4. Av(dB) = 20 log10(66.8) = 36.5 dB.

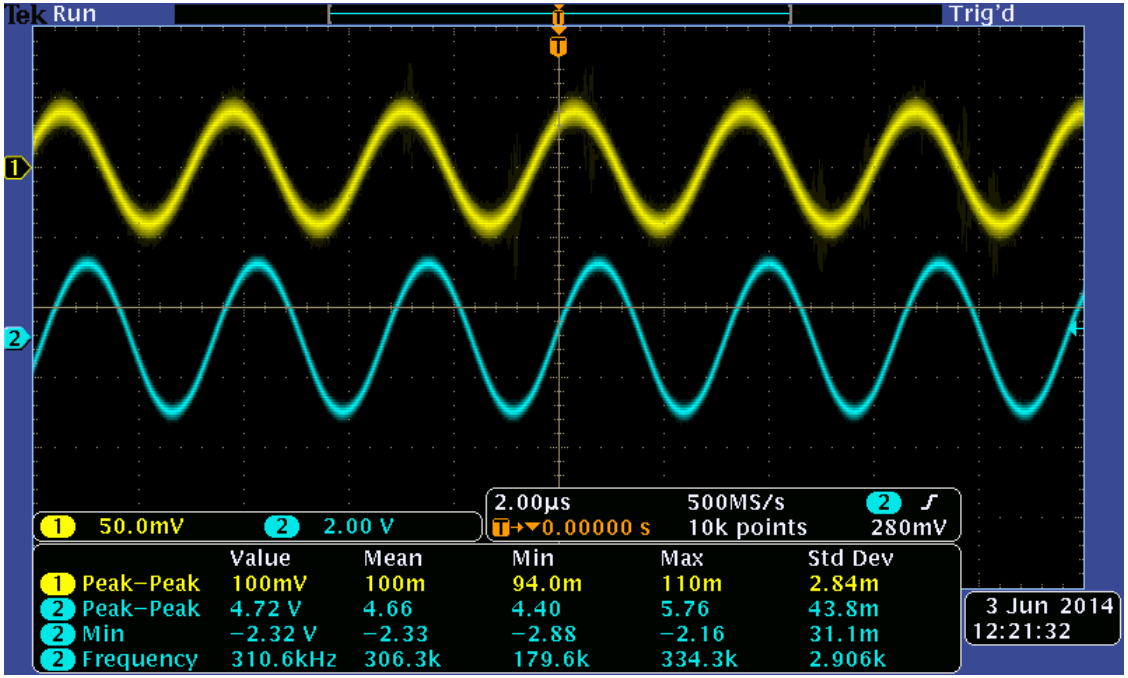




Measurements: Bandwidth

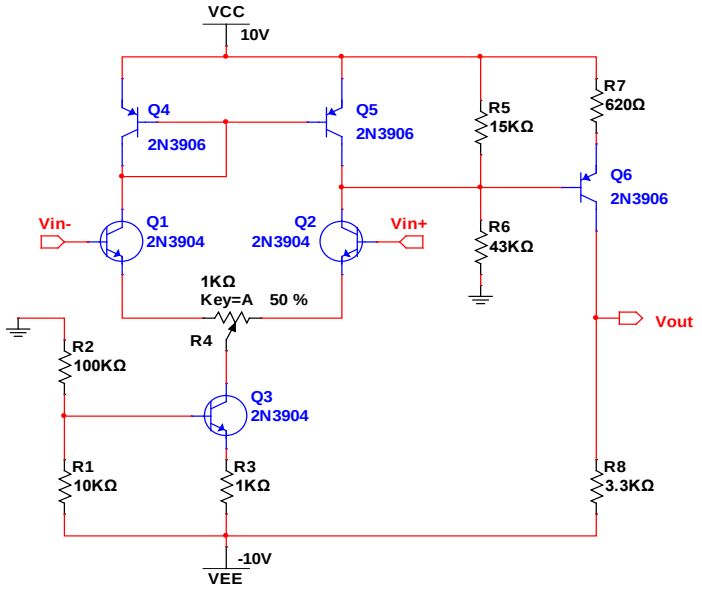
1. Increase the frequency of Vin+ until Av has fallen by 3 dB.
2. Capture an oscilloscope screenshot.
3. For me, Av = .7071 * 66.8 = 47.2. Shown here, Av = 47.2 at 310.6 KHz.



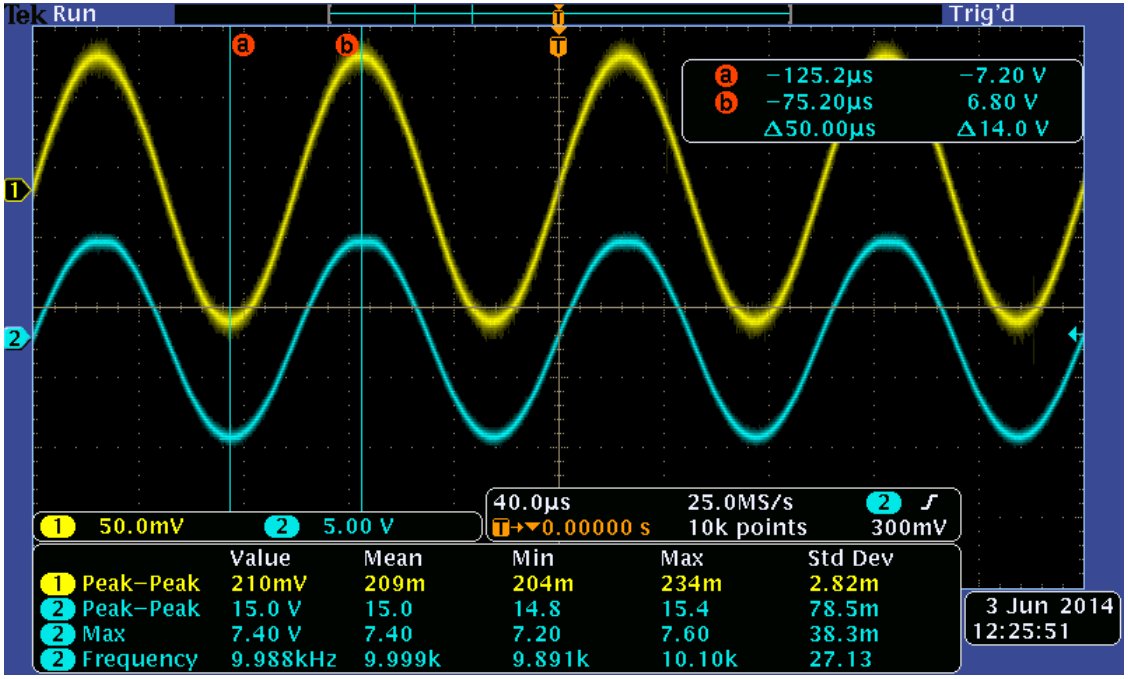


Measurements: Onset of clipping

1. Increase amplitude of Vin until onset of clipping.
2. Capture an oscilloscope screenshot.
3. For me, Vin = 209 mVpp.
4. Vout is clipping between 6.80 V (cursor) and 7.40 V (Max).

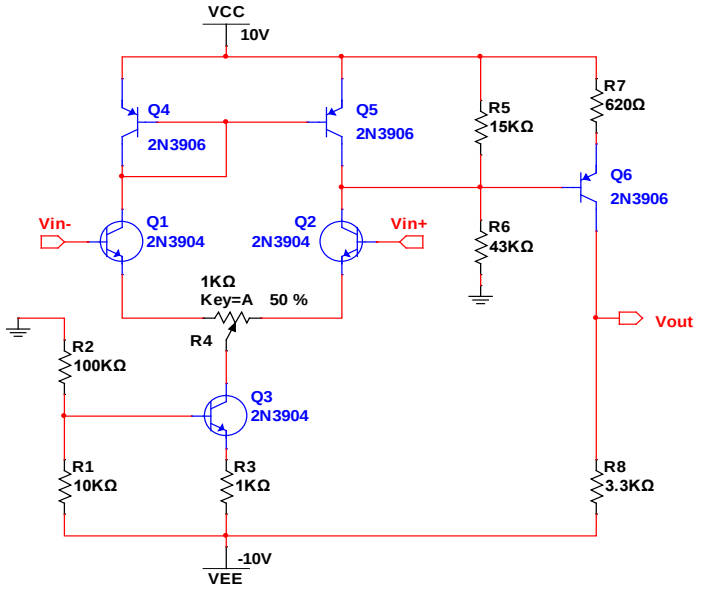


Clipping on the top happens when Q6 saturates.

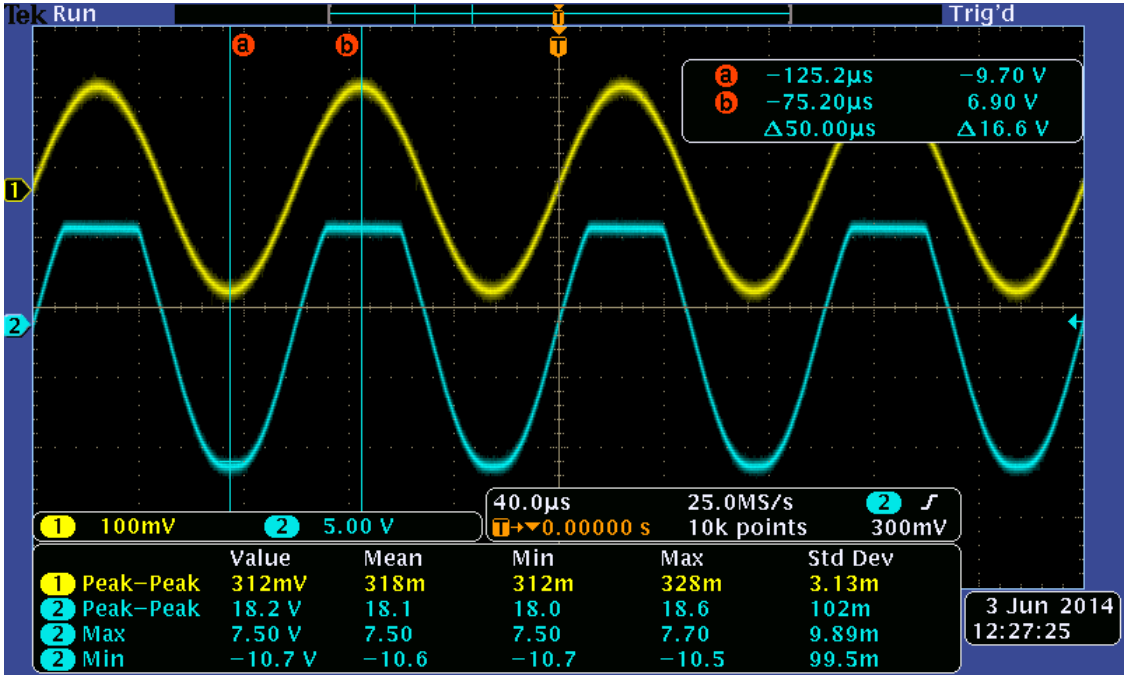


Measurements: Clipping both peaks

1. Increase amplitude of Vin until clipping both peaks.
2. Capture an oscilloscope screenshot.
3. For me, Vin = 318 mVpp.
4. Vout tops are clipping between 6.90 V (cursors) and 7.50 V (Max).
5. Bottoms are clipping between -9.70 (cursors) and -10.6 V (Min).



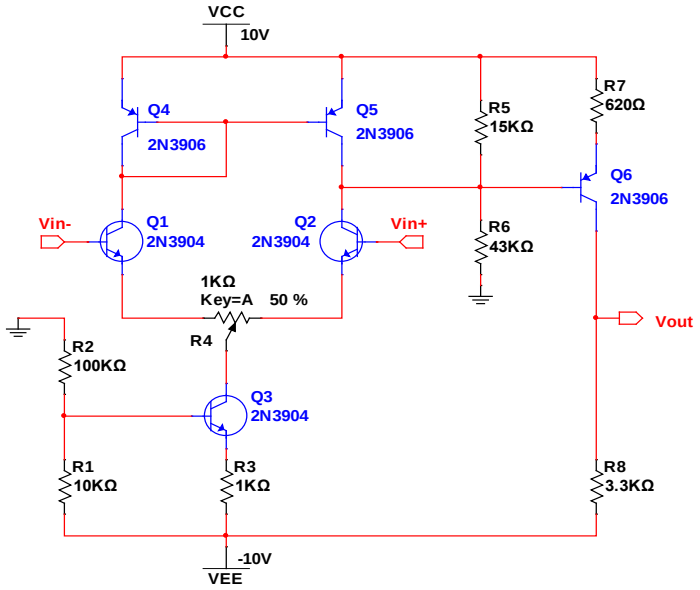
Clipping on the bottom happens when Q6 enters cutoff.

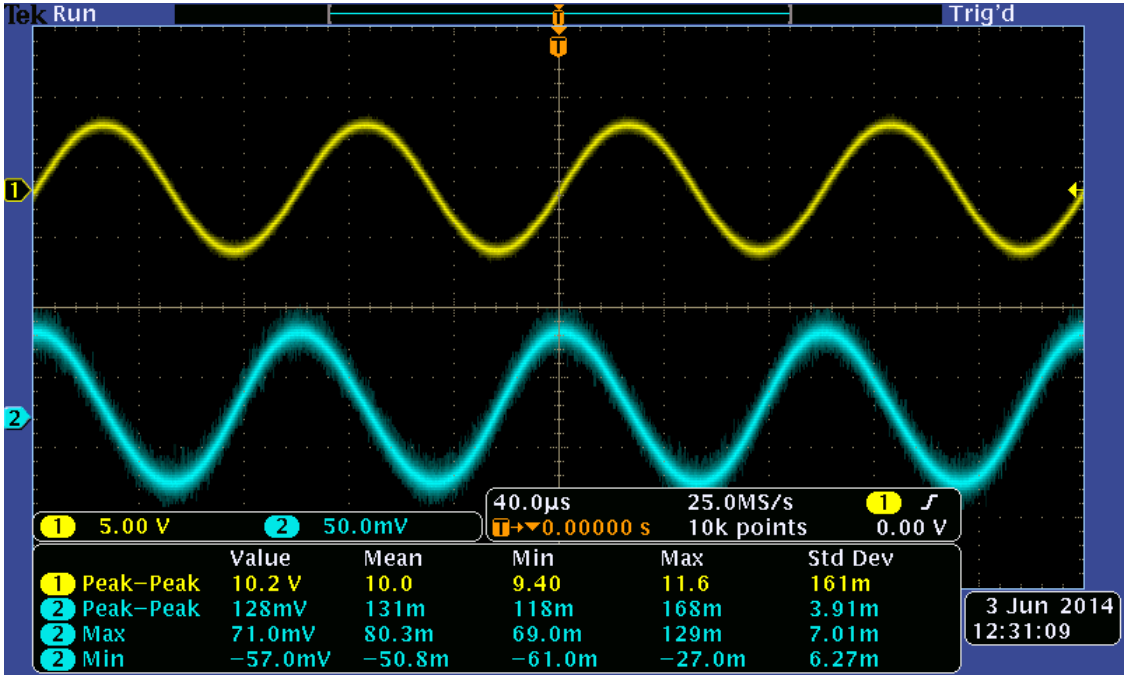


Measurements: Common mode

1. Set Vin– = Vin+ = 10 Vpp, 1.0 KHz sine wave, 0 V DC offset.
2. Shown here, Av(common mode) = 131 mVpp / 10.0 Vpp = .013.
3. Av(cm)dB = 20 log10(Av) = -37.7 dB

Common mode rejection ratio (CMRR)
= Av(dm in dB) – Av(cm in dB)
= 36.5 – (-37.7) = 74.2 dB





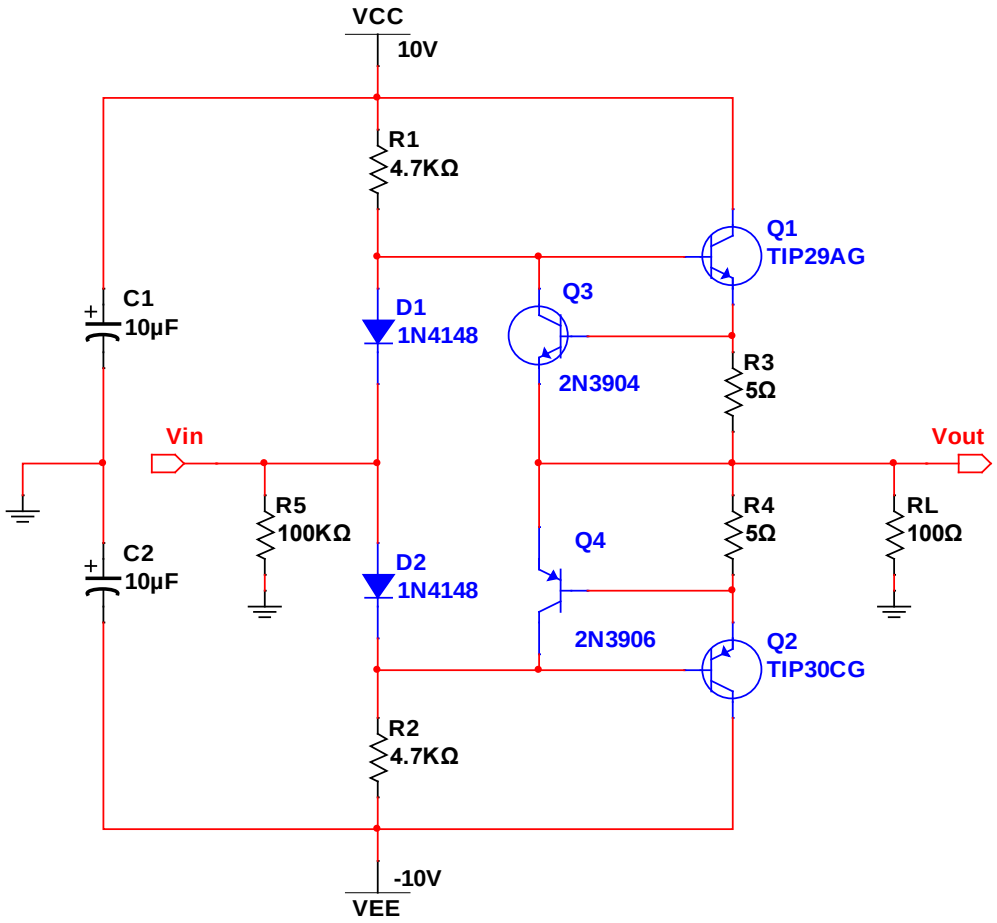
Complementary AB output stage.

The quiescent power dissipated in a transistor = IC * VCE at the Q-point.

One way to reduce quiescent power is by using two a complementary pair or NPN and PNP transistors.

At the Q-point, both transistors are off. Q1 turns on when Vin is positive and Q2 turns on if Vin is negative.

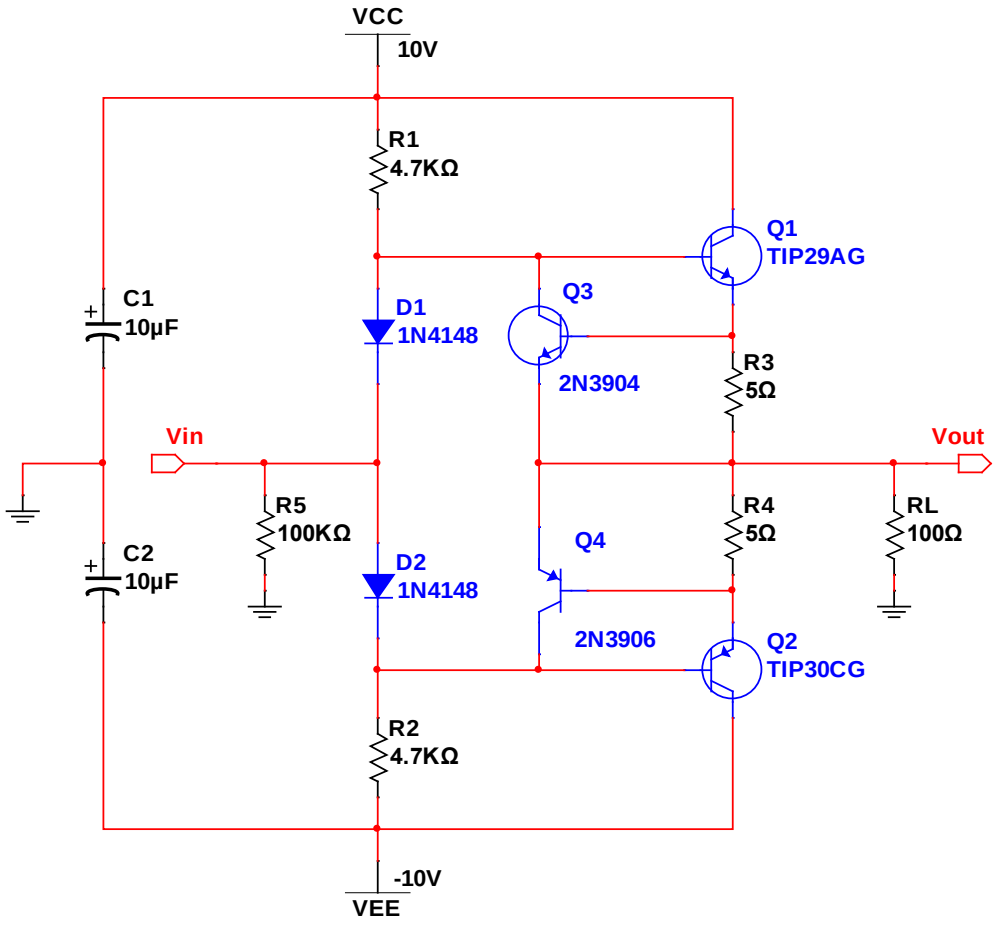
This is called class AB operation.



Use heat sinks on Q1 and Q2.

Short-circuit protection.

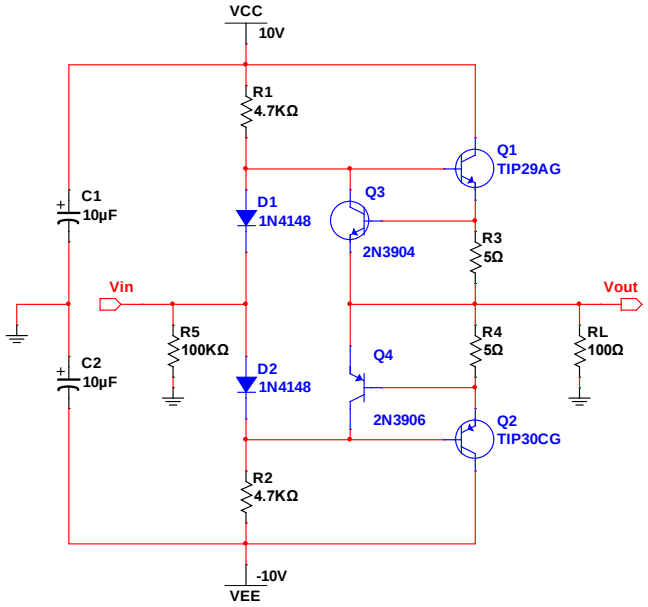
Q3 and Q4 provide short-circuit protection. When the voltage drop across either R 3 or R4 > 0.7 V, either Q3 or Q4 will turn on, dropping the base voltages VB1 or VB2, cutting them off.

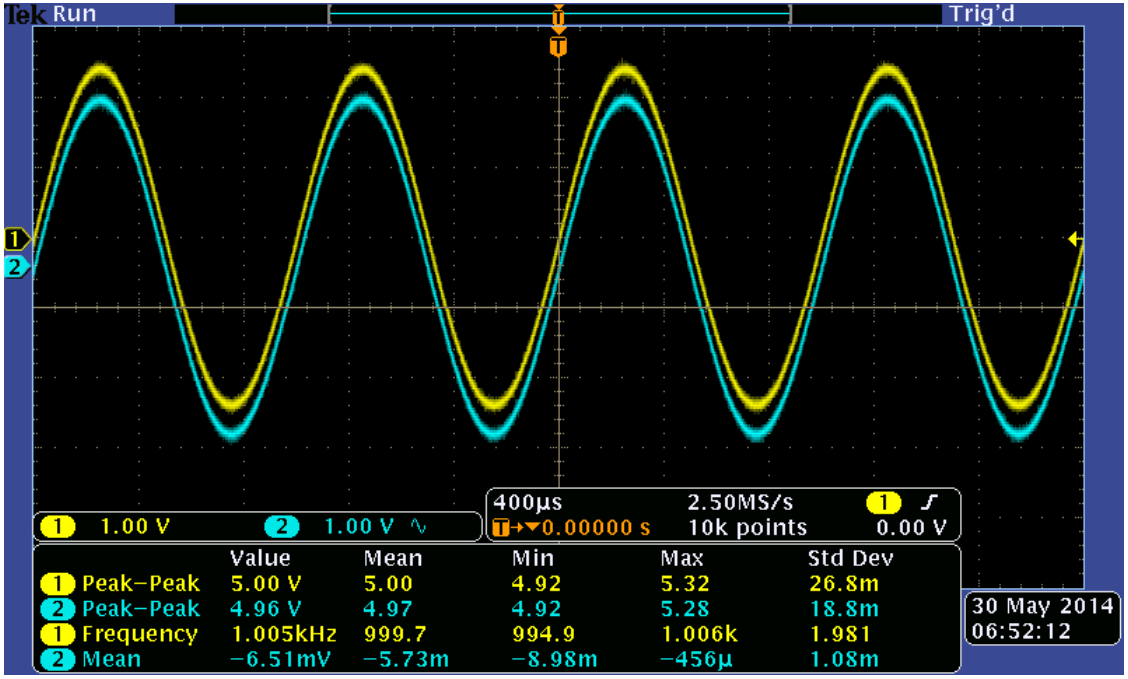


Use heat sinks on Q1 and Q2.

Measurements: Gain

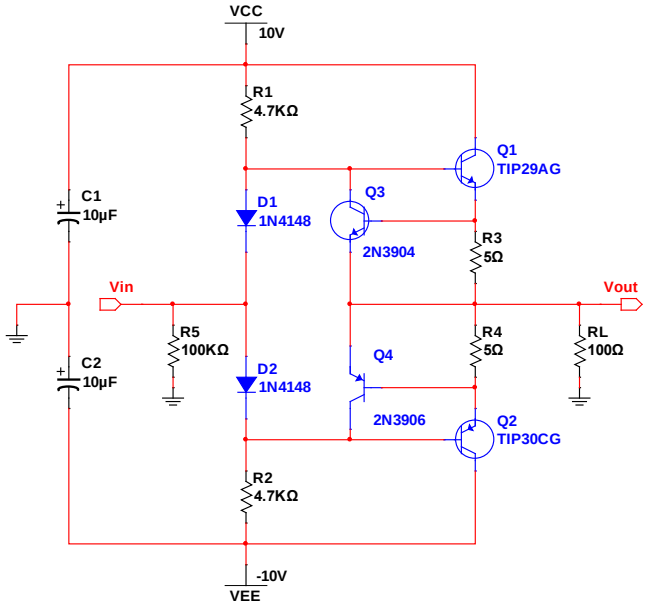
1. Set Vin = 5.0 Vpp, 1.0 kHz. Capture a screenshot and calculate Av.
2. Av = 4.97 / 5.00 = .99, just under unity, and non-inverting.
3. Vout has only a -5.7 mV DC offset.

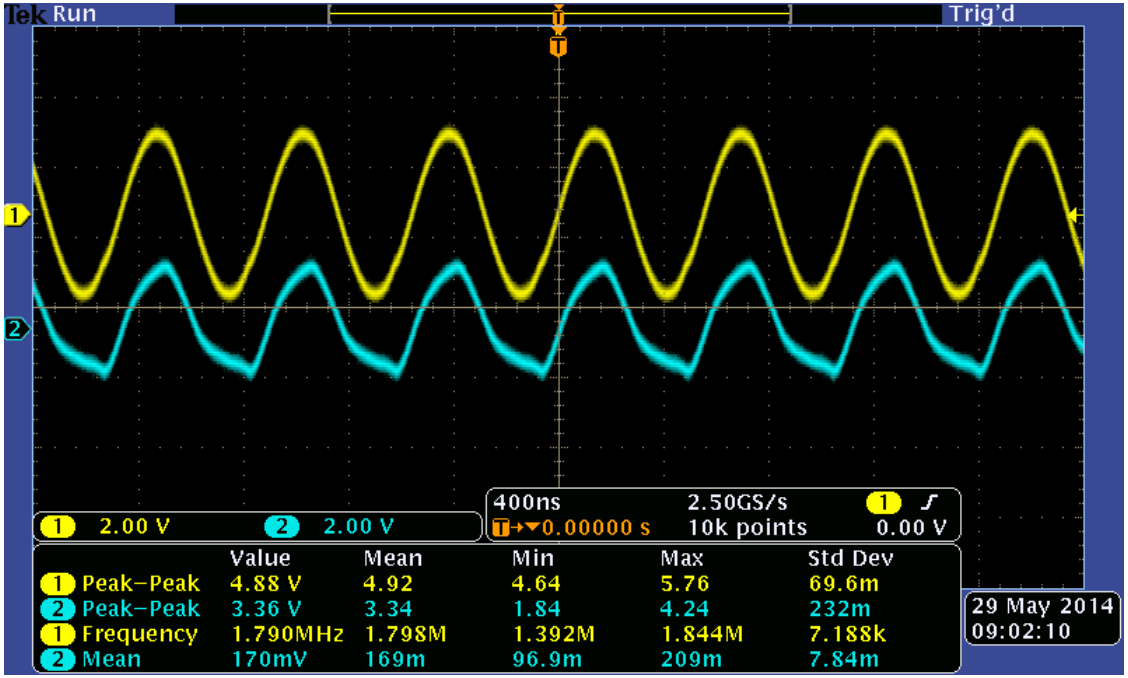




Measurements: Bandwidth

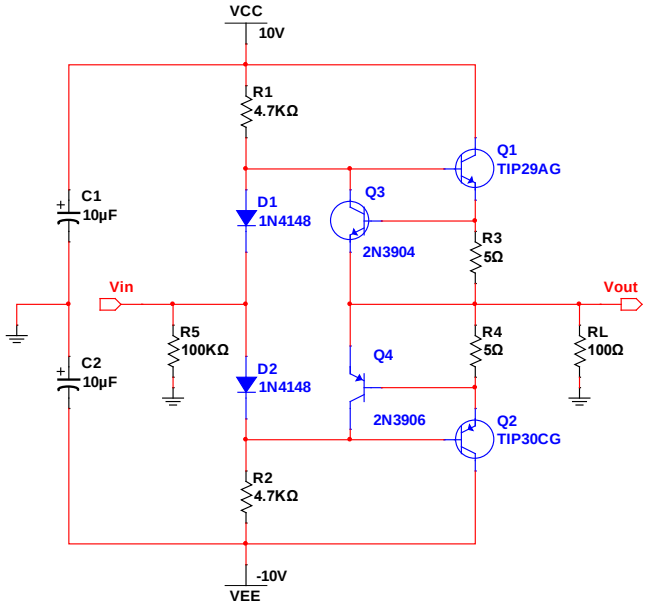
1. Find the 3 dB point. For my circuit, this would be where Av = .7071 * .99 = .70.
2. Shown here, Av = 3.34 / 4.92 = .68 at 1.8 MHz.
3. But note the distortion.

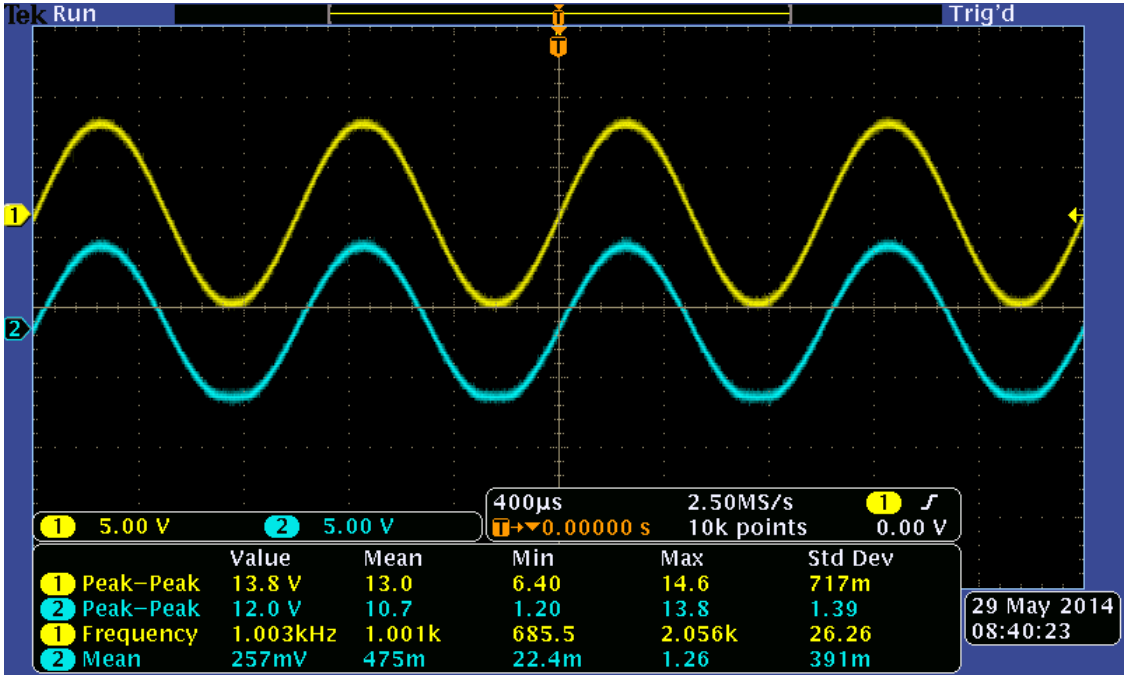




Measurements: Onset of clipping

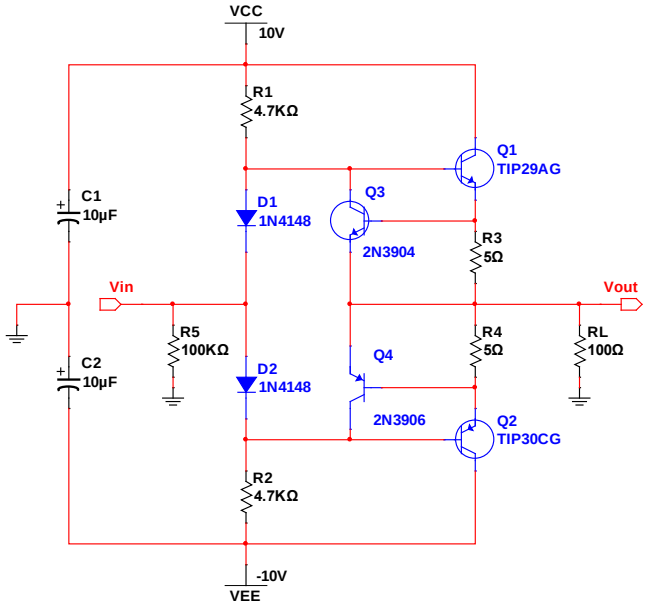
1. Reset Vin to 1.0 KHz and increase the amplitude until Vout begins clipping on either peak.
2. For me, clipping on negative peaks is at Vout = 10.7 Vpp.

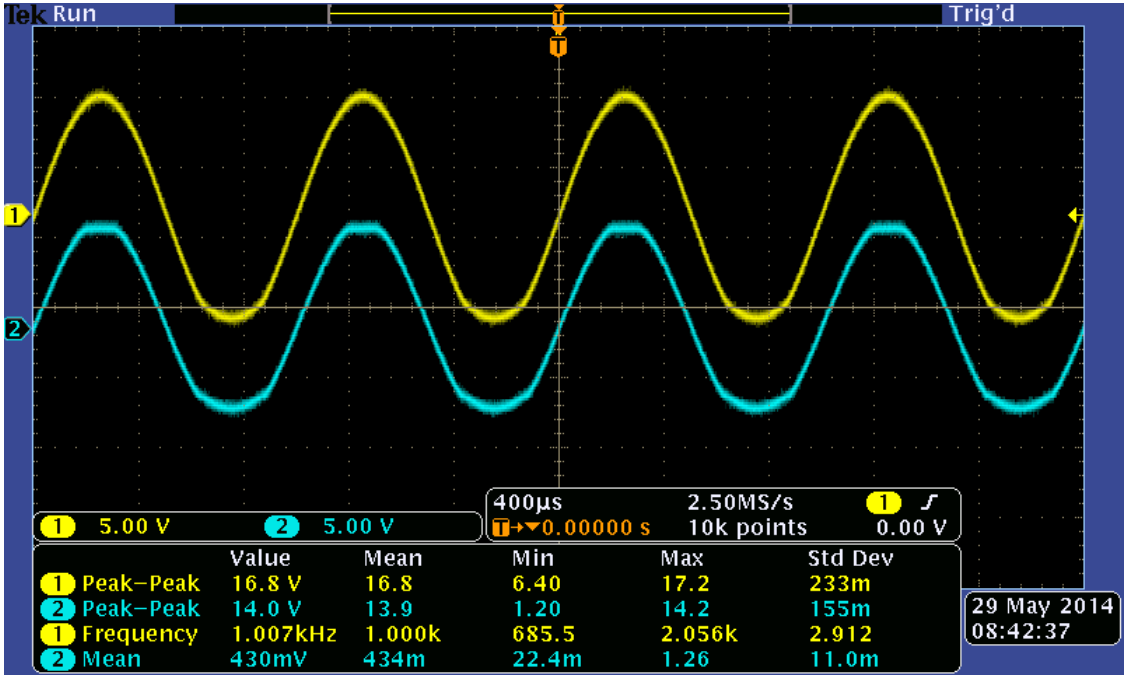




Measurements: Clipping both peaks

1. Continue increasing the amplitude of Vin until Vout begins clipping on the other peak.
2. For me, clipping on both peaks occurs at Vout = 13.9 Vpp..

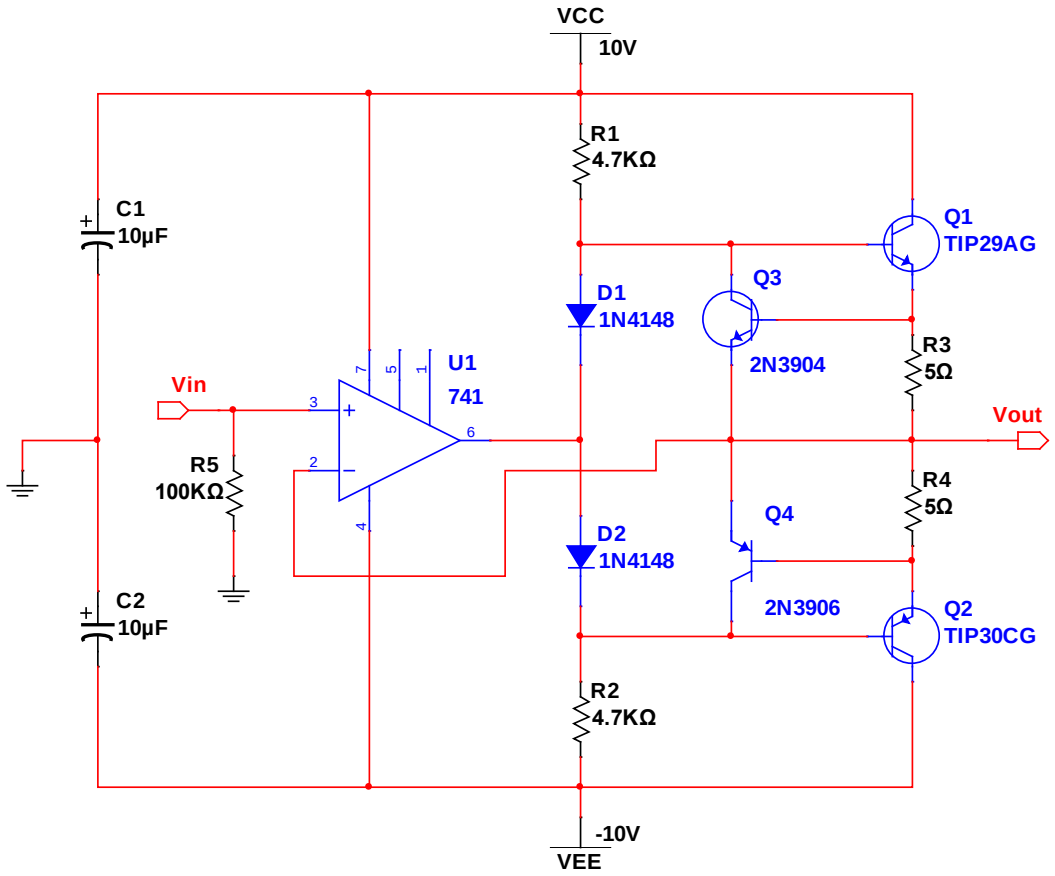




Multi-stage amplifier with feedback.

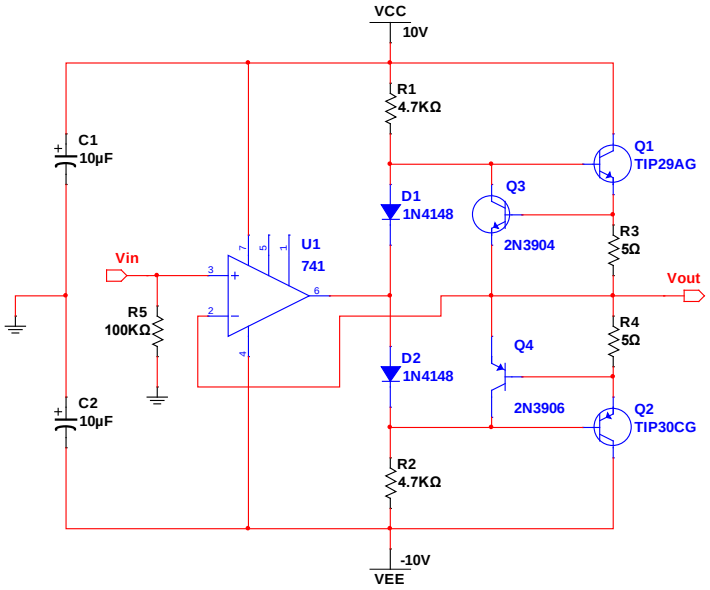
This circuit uses a commercial opamp front-end, mated to an AB output stage.

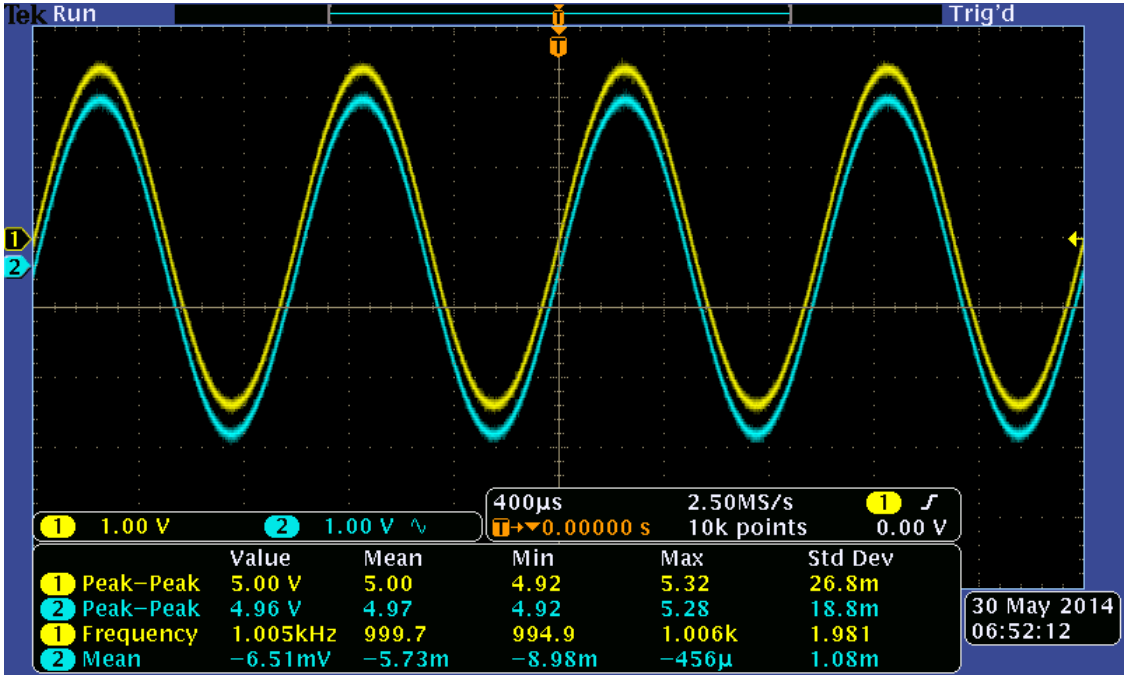
Negative feedback in this circuit ensures that Av = 1.



Measurements: Gain

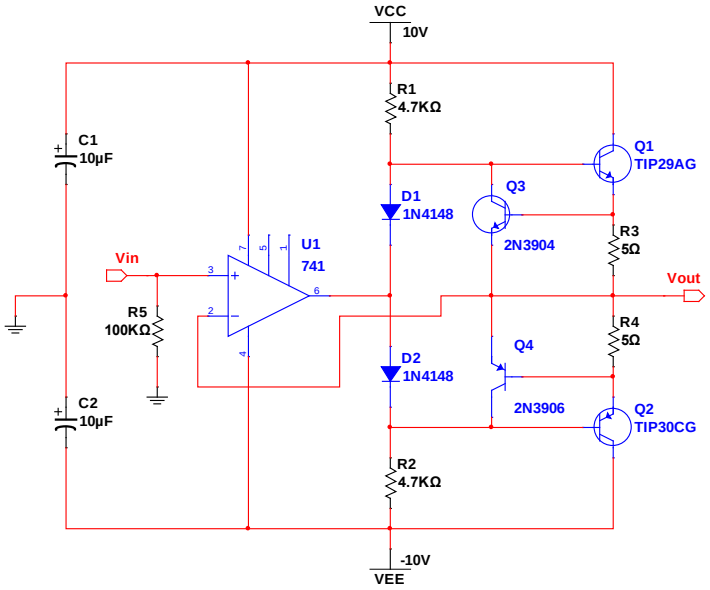
1. Set Vin = 5.0 Vpp, 1.0 kHz. Capture a screenshot and calculate Av.
2. Av = 4.97 / 5.00 = .99, just under unity, and non-inverting.
3. Vout has only a -5.7 mV DC offset.

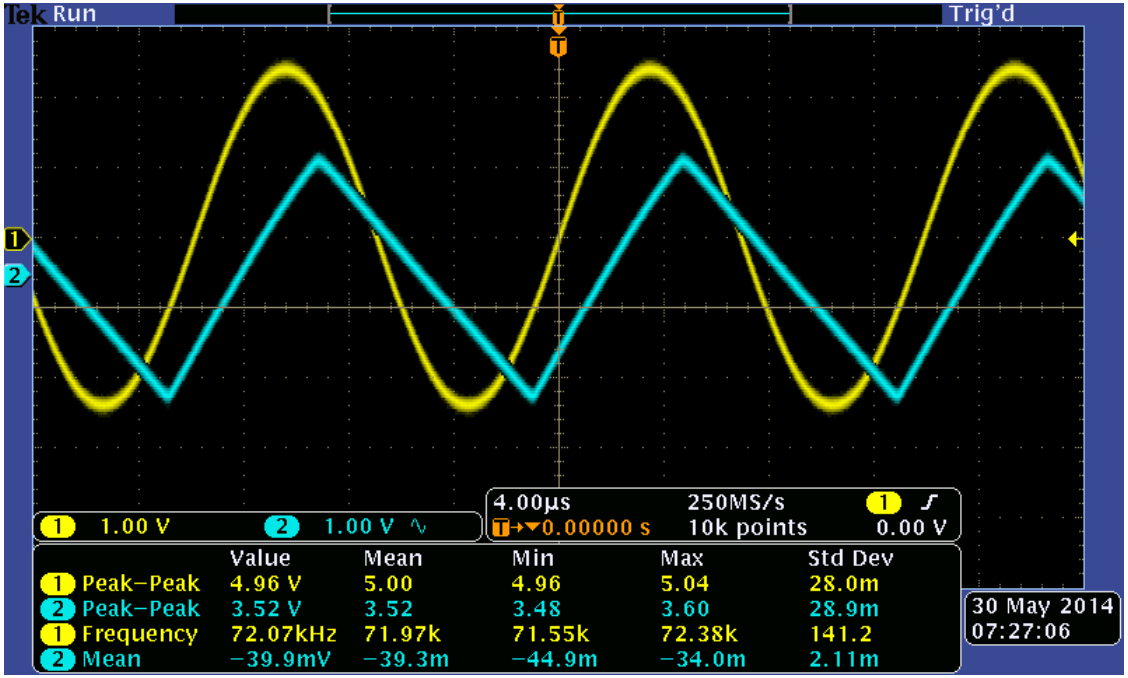




Measurements: Bandwidth

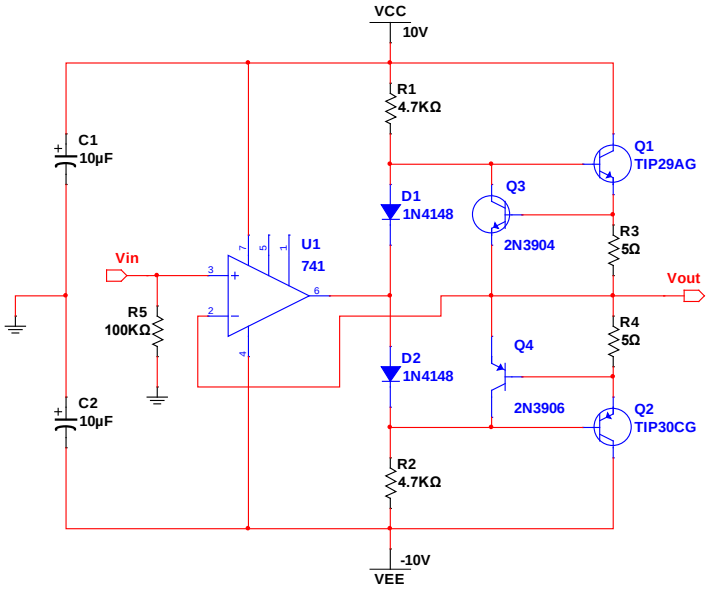
1. Find 3 dB point.
2. Shown here, Av = 3.52 / 5.00 = .704 at 72 KHz.
3. But note the distortion. The output is almost a triangle because we've hit the opamp's slew rate.

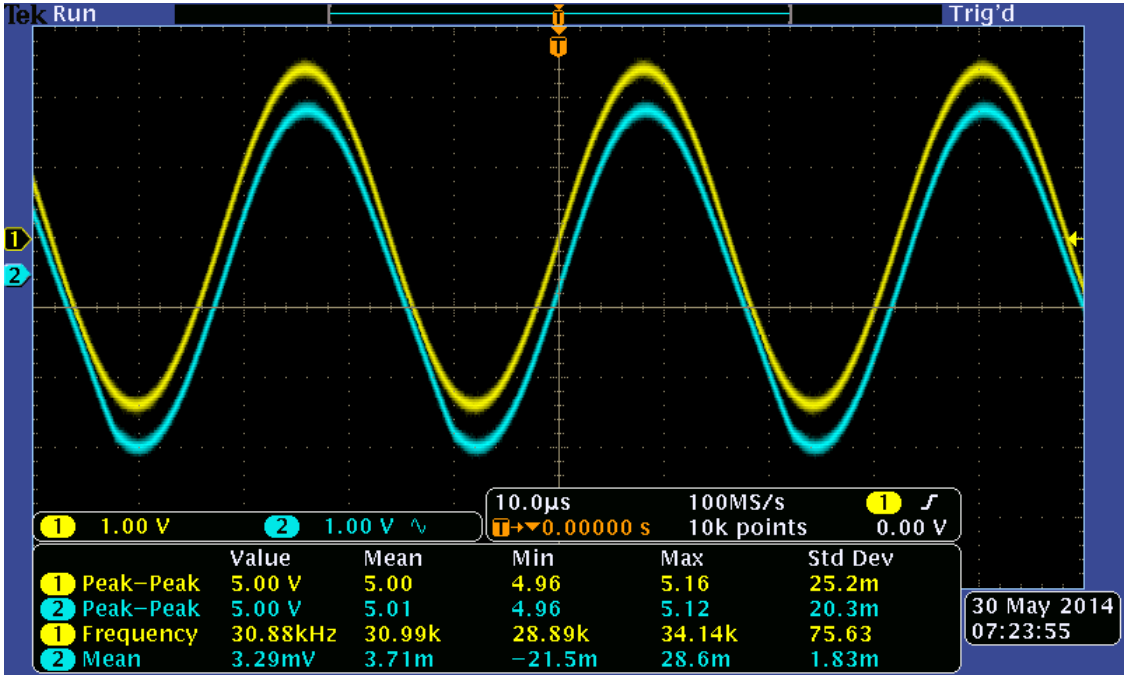




Onset of slew rate limitation.
(Not required.)

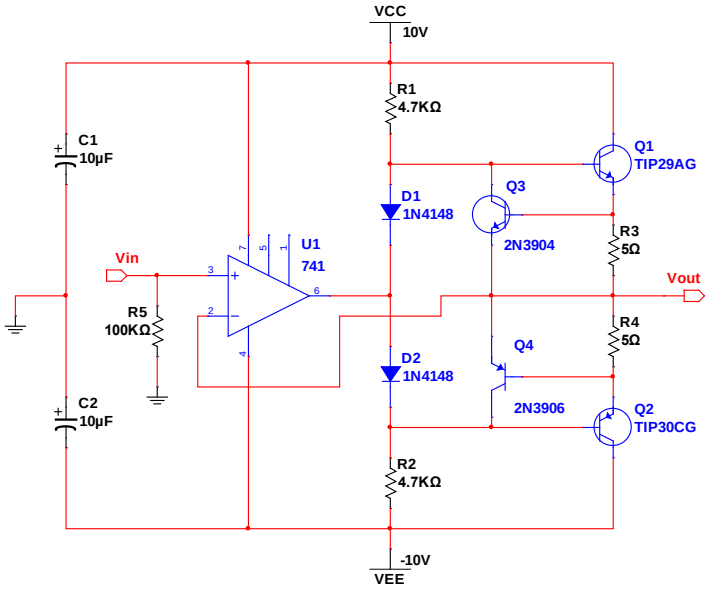
About 31 KHz for Vin = 5.0 Vpp.

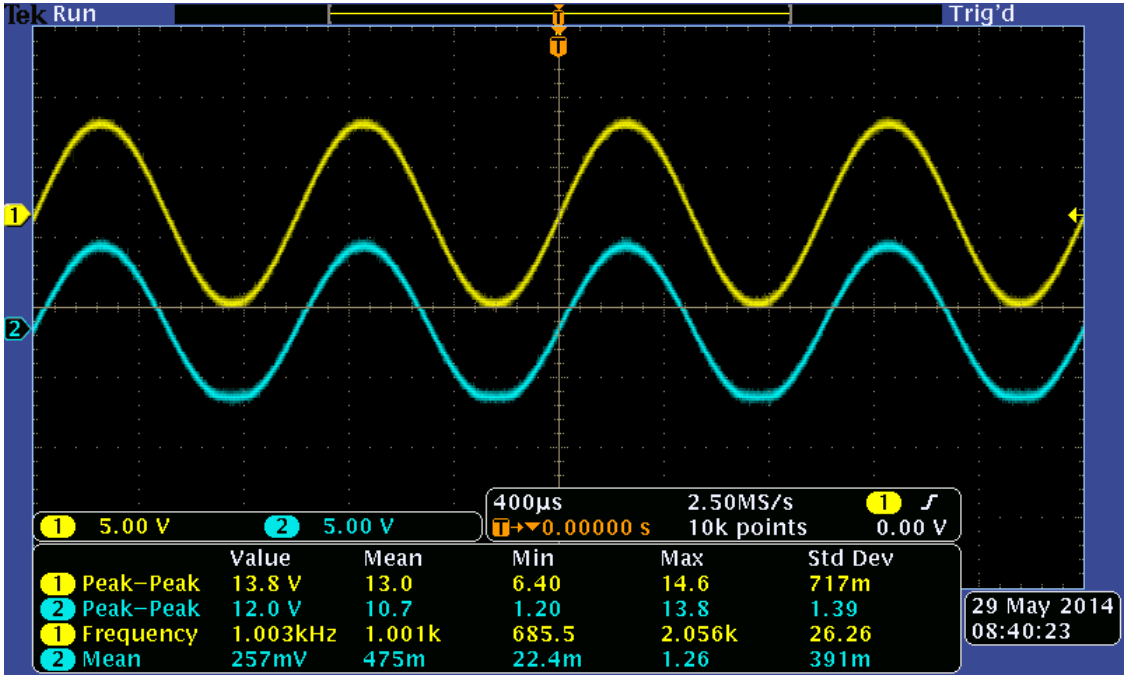




Measurements: Onset of clipping

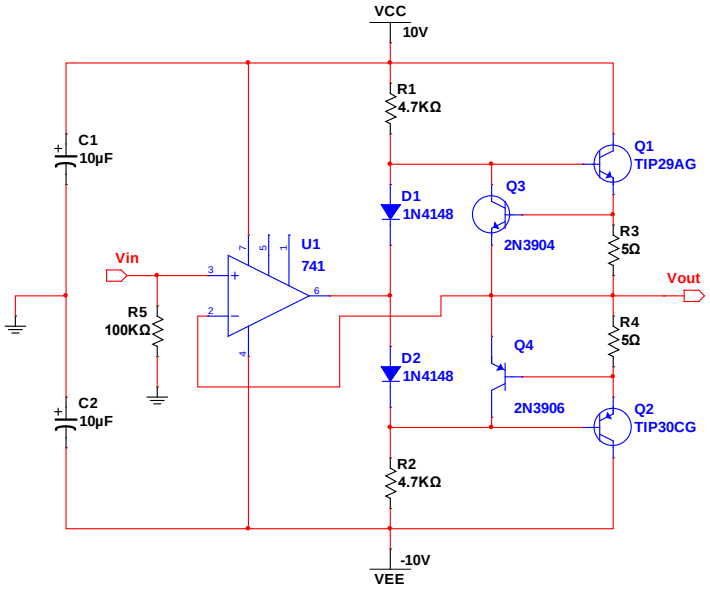
1. Increase Vin until clipping begins.
2. Shown here, it's clipping negative at Vin = 13 Vpp.

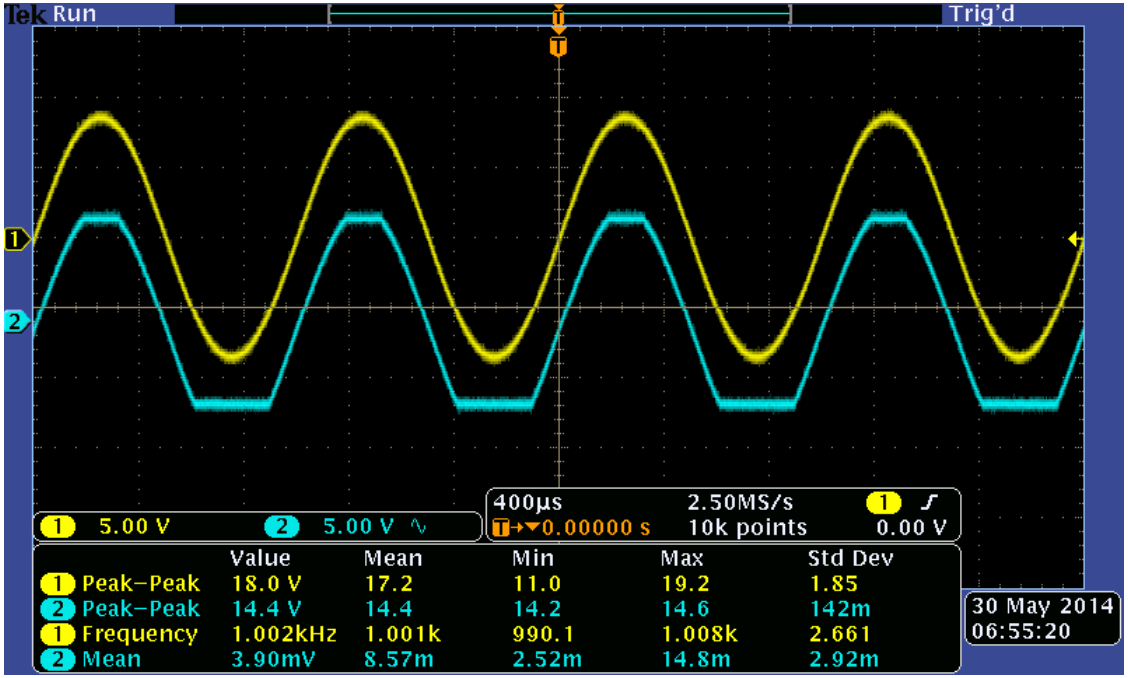




Measurements: Clipping both peaks

1. Increase Vin until clipping begins.
2. Shown here, it's clipping both peaks happens at Vin = 17 Vpp.





My results, comparing with and without the opamp front-end and feedback loop.

	Without opamp	With opamp
Vin Initial clipping	10.7 Vpp	13 Vpp
Vin Clipping both peaks	13.9 Vpp	17 Vpp
Bandwidth	1.8 MHz	72 KHz